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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,290	09/22/2003	Ingemar Soderquist	19391.0054	5630

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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,290	SODERQUIST ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 and 10 have been considered. Claims 8-9 have been cancelled as per Applicant's request. Claims 1-7 have been amended as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Knapp et al. (USPN 5,826,072, herein Knapp).

4. As per Claim 1, Knapp teaches: A digital signal processor comprising:

an instruction memory (Column 5, Lines 56-58), a central arithmetic unit (Column 6, Lines 10-12, the ALU), a register (Column 5, Lines 61-62), a controller (Column 5, Lines 62-63, the interrupt control logic), and input/output devices (Column 6, Line 1);

characterized in that

the instruction memory is arranged to include logical operations (Column 5, Lines 56-58), time performance constraints (Column 2, Lines 25-27) and events (Column 5, Line 64 – Column 6, Line 5);

the controller is arranged to suspend further processing of time performance constraints after initiating operations in an event control unit (Column 5, Line 64 –

Column 6, Line 5. For the remainder of this office action, it is assumed that the "event control unit" not only executes in a reaction to an event, but also is also the part of the processor that executes and/or schedules all instructions. This assumption is made by viewing Page 2, Lines 29-32 of the specification, where it appears that the event control unit is also responsible for executing or scheduling the "time performance constraints", in addition to the events. When the event (the interrupt in this case) is activated, it is run, and afterwards, the original instructions can resume running. By having to return to where the program was interrupted, it is clear that Knapp halts execution of the instruction flow during the interrupt) and resume processing when advised by the event control unit (Column 10, Lines 10-14, the return from interrupt instruction, where it has been stated above that the event control unit is interpreted to also include scheduling functions, such as scheduling a return from interrupt);

the event control unit is arranged to recognize an event that initiates processing by the event control unit, wherein the event is an input signal (Column 5, Lines 64-67, the signal is the interrupt request signal being activated) and to control processing to be carried out as a consequence of the event (Column 5, Line 64 – Column 6, Line 9. Also see Column 7, Lines 18-32) while fulfilling the time performance constraints (Column 6, Lines 3-5, it returns to the normal instruction flow (the time performance constraint instructions) when the event is finished), wherein a pulse package held in the event control unit includes an event operand operable to identify the input signal to initiate processing by the event control unit (Column 5, Lines 64-67) and a delay operand that defines a stop condition for a counter in the event control unit (Column 15, Lines 15-21,

interrupts are stopped for 4 clock cycles after an interrupt occurs, and a counter is inherent to be able to keep track of those cycles).

5. As per Claim 2, Knapp teaches: A digital signal processor in accordance with claim 1, wherein the event (Column 5, Lines 61-63. The interrupt control logic functions as a detector, as it receives interrupt request signals, and as shown in Column 6, Lines 2-5, responds to the event as a consequence of those signals being detected) is detected by the event control unit (Column 5, Line 64 – Column 6, Line 9).

6. As per Claim 3, Knapp teaches: A digital signal processor in accordance with claim 2, wherein the event control unit is arranged to detect input signals (inherent that the control logic would be able to differentiate between a logic "0" and "1" on a signal line).

7. As per Claim 4, Knapp teaches: A digital signal processor in accordance with claim 2, wherein a further event is recognized as a completion of the processing carried out as a consequence of a previous event (Column 10, Lines 11-14, where there needs to be an explicit signal (or instruction) to end an interrupt).

8. As per Claim 5, Knapp teaches: A digital signal processor in accordance with claim 1, wherein the event is recognized as a completion of the processing carried out as a consequence of a previous event (Column 10, Lines 11-14, where there needs to

be an explicit signal (or instruction) to end an interrupt).

9. As per Claim 6, Knapp teaches: A digital signal processor in accordance with claim 1, wherein the event control unit includes a signal memory arranged to store and extract data under control of the event control unit (Column 6, Lines 26-29, data memory 90).

As per Claim 7, Knapp teaches: A digital signal processor in accordance with claim 6, wherein the signal memory is a vector memory (Column 12, Lines 65-66 show that the memory can be a "vector memory").

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp, in view of Patterson et al. (herein Patterson).

12. As per Claim 10, Knapp teaches A digital signal processor in accordance with claim 1, but fails to teach: including two or more event control units arranged to work independently from each other.

However, Patterson teaches the idea of making a processor superscalar. A superscalar processor can execute multiple instructions at the same time, as long as they remain independent of each other (Pages 278-279). As assumed in the Claim 1 rejection, an "event control unit" appears to be a general execution unit, as it appears to work on all kinds of instructions in the processor. As shown in Patterson, and as one of ordinary skill in the art would recognize, the advantage of parallel processing is to increase performance by decreasing the cycles per instruction of the processor (Page 278). Given this advantage, it would have been obvious to one of ordinary skill in the art to apply the knowledge of superscalar processors to Knapps invention, and apply the same mechanic to the event control units, to allow for multiple units to execute simultaneously and independently for increased overall performance.

Response to Arguments

13. Examiner acknowledges the new drawings, which overcome the objections in the previous Office Action, which have been withdrawn. Likewise, the objections to the specification have been overcome by the amendments to the specification.

14. Examiner further acknowledges the amendments to the claims overcome the objections to Claims 1 and 5, and overcome the 112 rejections to Claims 3 and 7-9 (of which 8 and 9 were cancelled).

15. Applicant's arguments filed 8/30/2006 have been fully considered but they are not persuasive. Applicant has essentially argued that the additional limitations to the event control unit in Claim 1 overcome the teachings in Knapp, namely, resuming processing when advised by the unit, initiating processing on an input signal, and a "pulse package", including an operand operable to identify the input signal, and a delay operand to define a stop condition for a counter. As Examiner stated in the previous Office Action, the Examiner considers the event control unit as taught by Knapp to not only be the part of the system which executes the interrupt, but also the part which helps schedule instructions, and with that in mind, the Examiner traverses the new limitations. Regarding resuming processing when advised by the event control unit, given that the event control unit is interpreted to include a scheduling mechanism, and that Knapp resumes processing when a return from interrupt instruction is processed (Column 10, Lines 10-14), Knapp reads on this limitation. Regarding initiating processing by recognizing an event, which is an input signal, Knapp, in Column 5, Lines 64-67 shows that Knapp initiates an interrupt when an interrupt request signal is activated. Regarding a "pulse package", while Knapp does not teach an explicit "pulse package", a pulse package has not been described in any detail other than its contents, of which Knapp has equivalent functionality, thus the package has been treated as an

abstract idea for the functionality it describes. As for an event operand operable to identify the input signal to initiate processing, Examiner refers back to Column 5, Lines 64-67, the interrupt request signal, if activating this signal triggers an interrupt, then there must be something to identify and check that signal. Regarding a delay operand to define a stop condition for a counter, Knapp teaches in Column 15, Lines 15-21 that after an interrupt is processed, no other interrupts can be triggered for 4 (or more) clock cycles. In order to keep track of clock cycles, a counter would be needed, after the 4 clock cycles are expired, the event control unit can process interrupts again, thus the stop condition would be the number of clock cycles until interrupts could begin again, with the counter stopped/reset, thus teaching the "delay operand" as disclosed by the claim.

Therefore, Knapp continues to teach the limitations of Claim 1, and the further dependant claims 2-6 and 10.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
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